FIG. 1

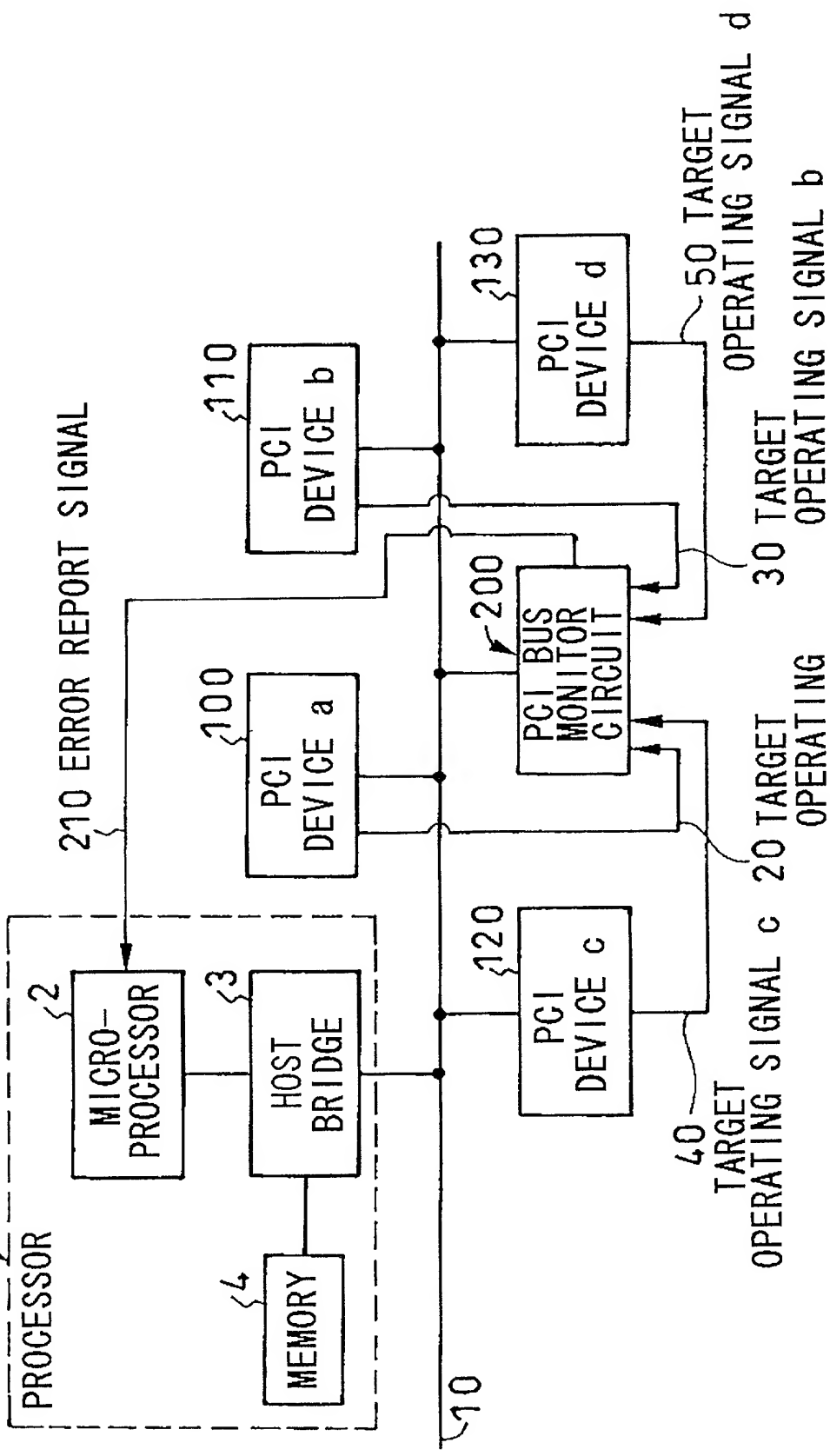

1
PROCESSOR
2
MICRO-PROCESSOR
3
HOST BRIDGE
4
MEMORY
10
210 ERROR REPORT SIGNAL
100
PCI DEVICE a
110
PCI DEVICE b
120
PCI DEVICE c
130
PCI DEVICE d
200
PCI BUS MONITOR CIRCUIT
20 TARGET OPERATING SIGNAL a
30 TARGET OPERATING SIGNAL b
40 TARGET OPERATING SIGNAL c
50 TARGET OPERATING SIGNAL d

FIG. 2

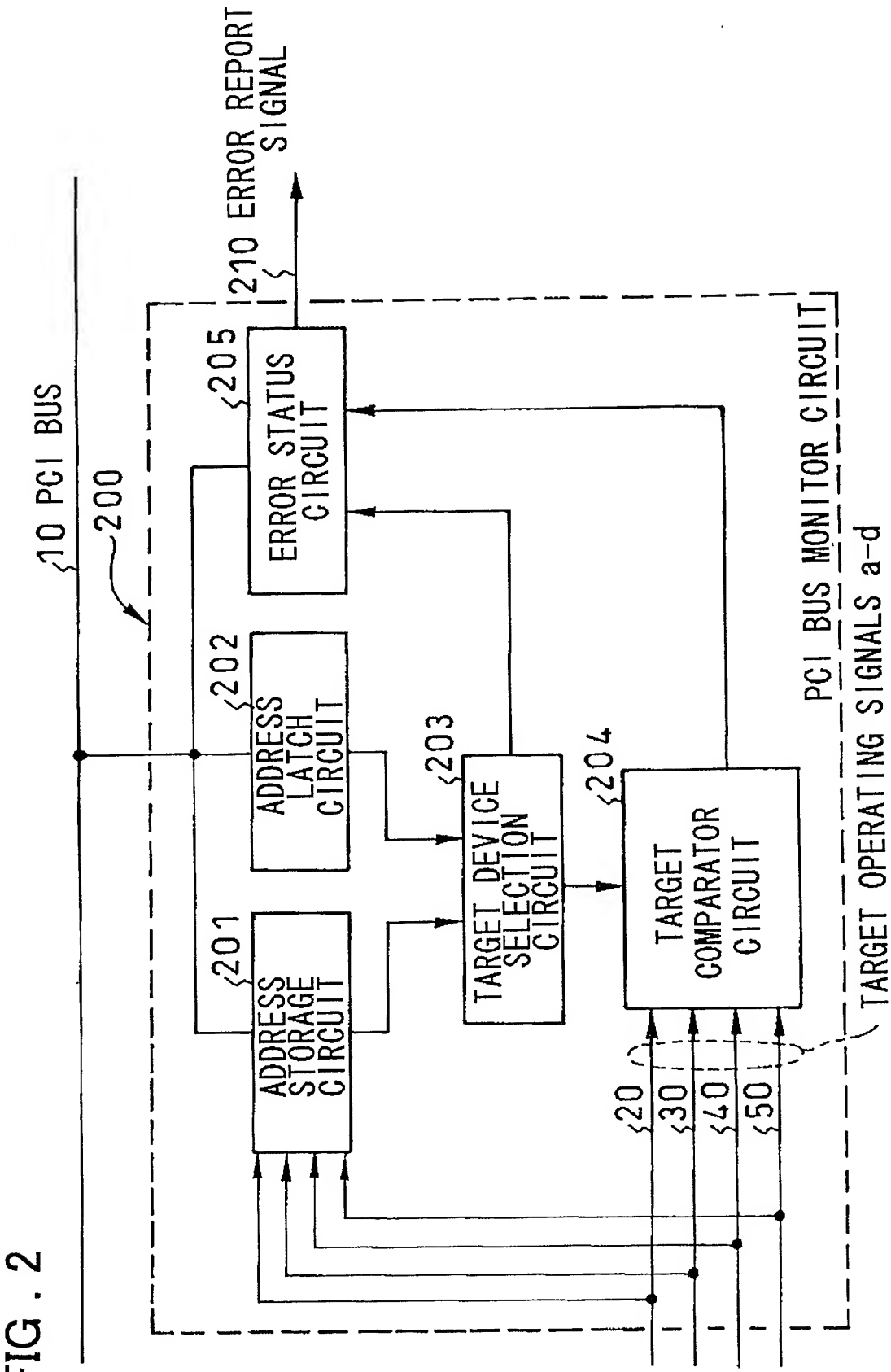

10 PCI BUS
200
210 ERROR REPORT SIGNAL
205
ERROR STATUS CIRCUIT
202
ADDRESS LATCH CIRCUIT
203
TARGET DEVICE SELECTION CIRCUIT
204
TARGET COMPARATOR CIRCUIT
201
ADDRESS STORAGE CIRCUIT
PCI BUS MONITOR CIRCUIT
TARGET OPERATING SIGNALS a-d
20
30
40
50

FIG . 3

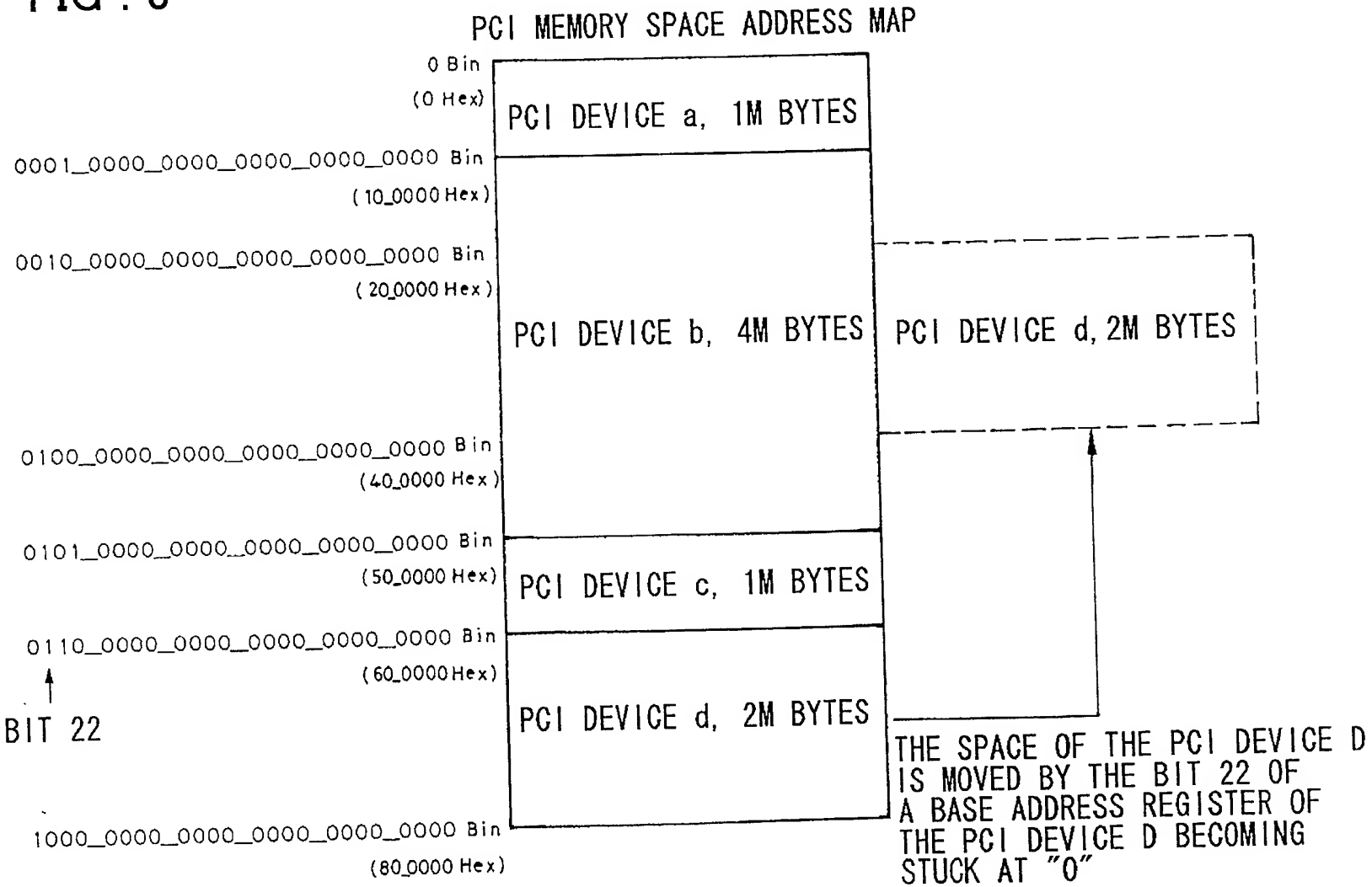

PCI MEMORY SPACE ADDRESS MAP
0 Bin
(0 Hex)
PCI DEVICE a, 1M BYTES
0001_0000_0000_0000_0000_0000 Bin
(10_0000 Hex)
0010_0000_0000_0000_0000_0000 Bin
(20_0000 Hex)
PCI DEVICE b, 4M BYTES
PCI DEVICE d, 2M BYTES
0100_0000_0000_0000_0000_0000 Bin
(40_0000 Hex)
0101_0000_0000_0000_0000_0000 Bin
(50_0000 Hex)
PCI DEVICE c, 1M BYTES
0110_0000_0000_0000_0000_0000 Bin
(60_0000 Hex)
BIT 22
PCI DEVICE d, 2M BYTES
1000_0000_0000_0000_0000_0000 Bin
(80_0000 Hex)
THE SPACE OF THE PCI DEVICE D IS MOVED BY THE BIT 22 OF A BASE ADDRESS REGISTER OF THE PCI DEVICE D BECOMING STUCK AT "0"

FIG . 4

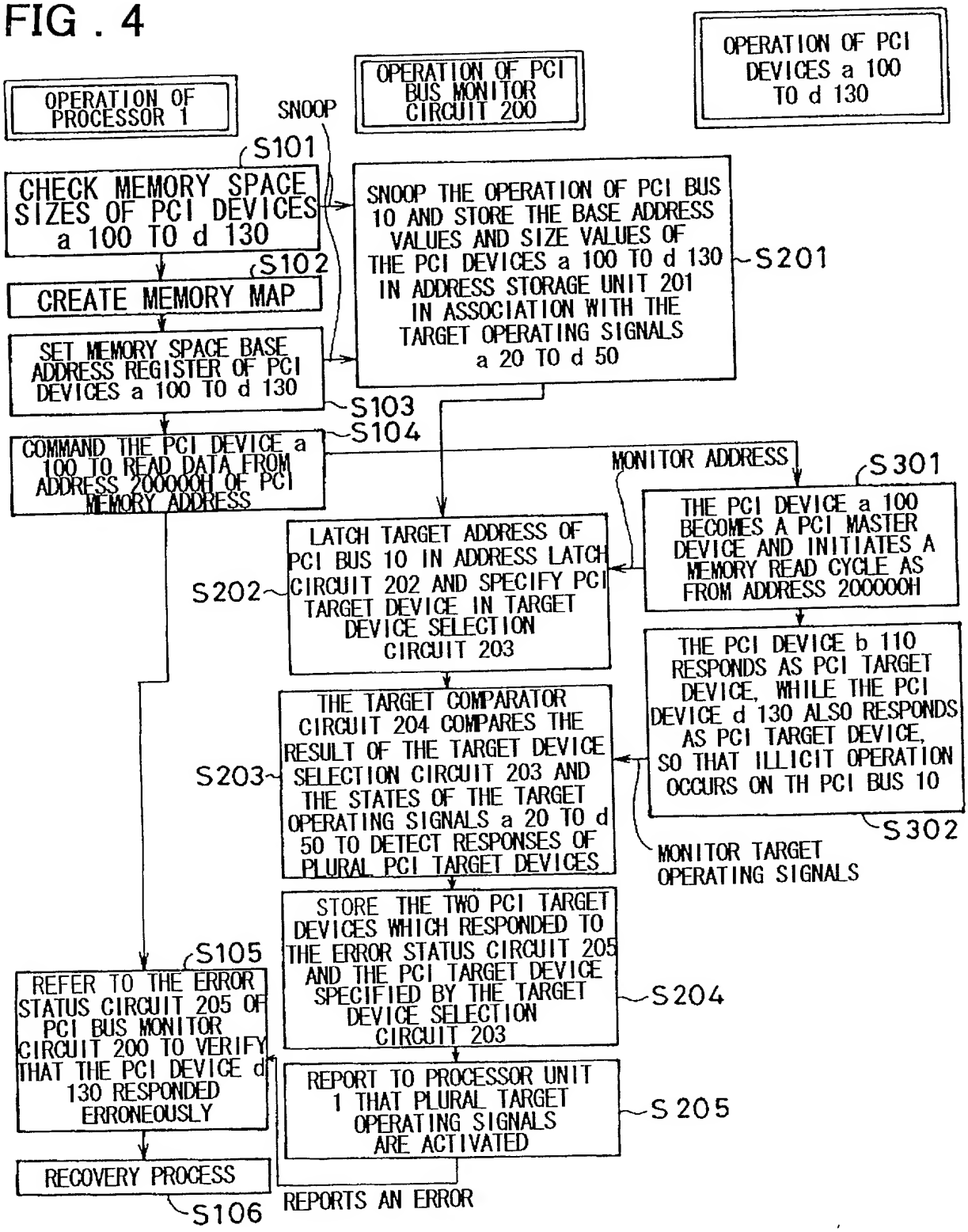

OPERATION OF PROCESSOR 1
OPERATION OF PCI BUS MONITOR CIRCUIT 200
OPERATION OF PCI DEVICES a 100 TO d 130
SNOOP
S101
CHECK MEMORY SPACE SIZES OF PCI DEVICES a 100 TO d 130
S102
CREATE MEMORY MAP
SET MEMORY SPACE BASE ADDRESS REGISTER OF PCI DEVICES a 100 TO d 130
S103
S104
COMMAND THE PCI DEVICE a 100 TO READ DATA FROM ADDRESS 200000H OF PCI MEMORY ADDRESS
SNOOP THE OPERATION OF PCI BUS 10 AND STORE THE BASE ADDRESS VALUES AND SIZE VALUES OF THE PCI DEVICES a 100 TO d 130 IN ADDRESS STORAGE UNIT 201 IN ASSOCIATION WITH THE TARGET OPERATING SIGNALS a 20 TO d 50
S201
MONITOR ADDRESS
S301
THE PCI DEVICE a 100 BECOMES A PCI MASTER DEVICE AND INITIATES A MEMORY READ CYCLE AS FROM ADDRESS 200000H
LATCH TARGET ADDRESS OF PCI BUS 10 IN ADDRESS LATCH CIRCUIT 202 AND SPECIFY PCI TARGET DEVICE IN TARGET DEVICE SELECTION CIRCUIT 203
S202
THE PCI DEVICE b 110 RESPONDS AS PCI TARGET DEVICE, WHILE THE PCI DEVICE d 130 ALSO RESPONDS AS PCI TARGET DEVICE, SO THAT ILLICIT OPERATION OCCURS ON TH PCI BUS 10
S302
THE TARGET COMPARATOR CIRCUIT 204 COMPARES THE RESULT OF THE TARGET DEVICE SELECTION CIRCUIT 203 AND THE STATES OF THE TARGET OPERATING SIGNALS a 20 TO d 50 TO DETECT RESPONSES OF PLURAL PCI TARGET DEVICES
S203
MONITOR TARGET OPERATING SIGNALS
STORE THE TWO PCI TARGET DEVICES WHICH RESPONDED TO THE ERROR STATUS CIRCUIT 205 AND THE PCI TARGET DEVICE SPECIFIED BY THE TARGET DEVICE SELECTION CIRCUIT 203
S204
S105
REFER TO THE ERROR STATUS CIRCUIT 205 OF PCI BUS MONITOR CIRCUIT 200 TO VERIFY THAT THE PCI DEVICE d 130 RESPONDED ERRONEOUSLY
REPORT TO PROCESSOR UNIT 1 THAT PLURAL TARGET OPERATING SIGNALS ARE ACTIVATED
S205
RECOVERY PROCESS
S106
REPORTS AN ERROR

FIG. 5

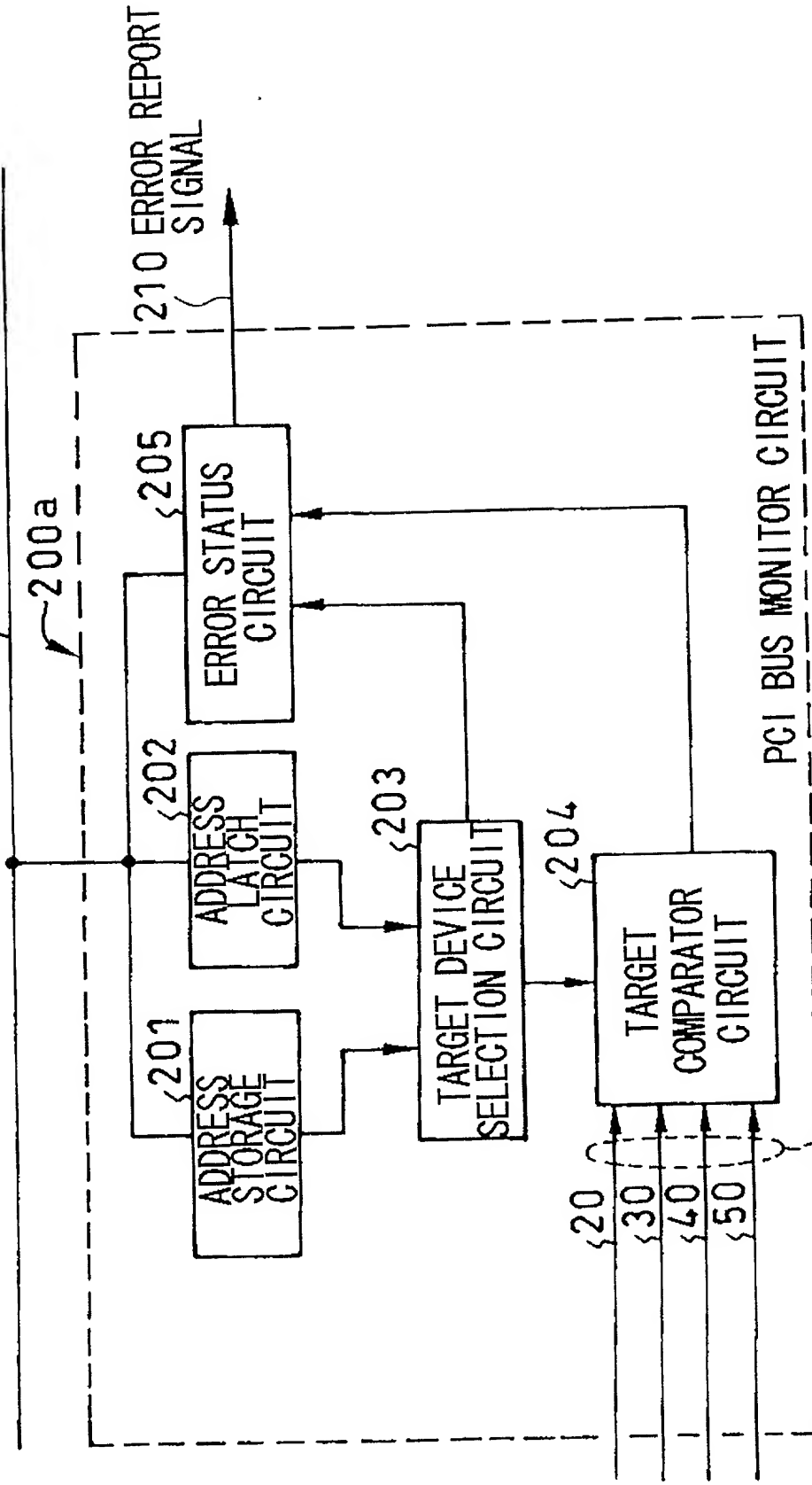

10 PCI BUS
200a
210 ERROR REPORT SIGNAL
205
ERROR STATUS CIRCUIT
202
ADDRESS LATCH CIRCUIT
203
TARGET DEVICE SELECTION CIRCUIT
204
TARGET COMPARATOR CIRCUIT
201
ADDRESS STORAGE CIRCUIT
PCI BUS MONITOR CIRCUIT
20
30
40
50
TARGET OPERATING SIGNALS a - d

FIG . 6

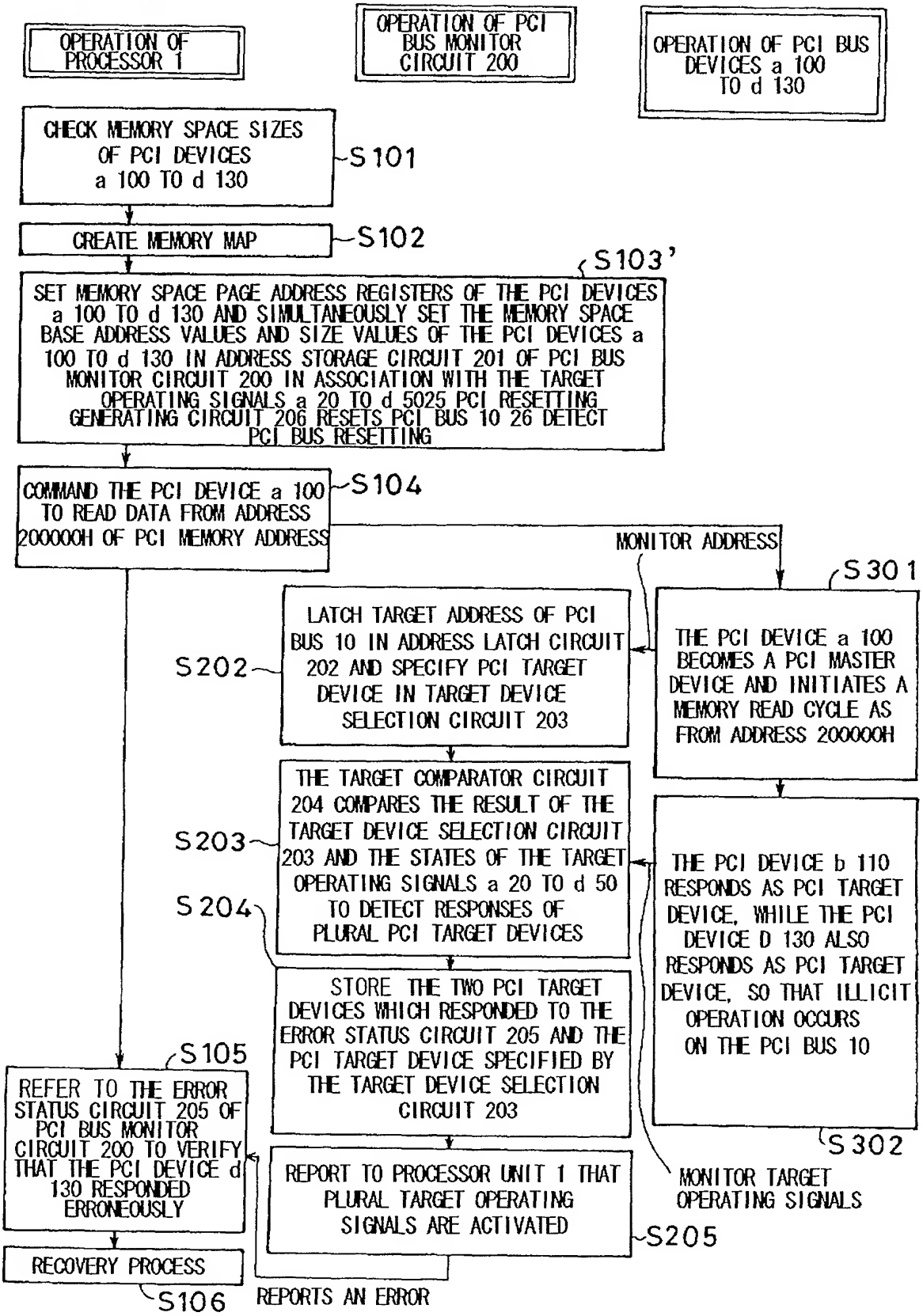

OPERATION OF PROCESSOR 1
OPERATION OF PCI BUS MONITOR CIRCUIT 200
OPERATION OF PCI BUS DEVICES a 100 TO d 130
CHECK MEMORY SPACE SIZES OF PCI DEVICES a 100 TO d 130
S101
CREATE MEMORY MAP
S102
S103'
SET MEMORY SPACE PAGE ADDRESS REGISTERS OF THE PCI DEVICES a 100 TO d 130 AND SIMULTANEOUSLY SET THE MEMORY SPACE BASE ADDRESS VALUES AND SIZE VALUES OF THE PCI DEVICES a 100 TO d 130 IN ADDRESS STORAGE CIRCUIT 201 OF PCI BUS MONITOR CIRCUIT 200 IN ASSOCIATION WITH THE TARGET OPERATING SIGNALS a 20 TO d 5025 PCI RESETTING GENERATING CIRCUIT 206 RESETS PCI BUS 10 26 DETECT PCI BUS RESETTING
COMMAND THE PCI DEVICE a 100 TO READ DATA FROM ADDRESS 200000H OF PCI MEMORY ADDRESS
S104
MONITOR ADDRESS
S301
THE PCI DEVICE a 100 BECOMES A PCI MASTER DEVICE AND INITIATES A MEMORY READ CYCLE AS FROM ADDRESS 200000H
LATCH TARGET ADDRESS OF PCI BUS 10 IN ADDRESS LATCH CIRCUIT 202 AND SPECIFY PCI TARGET DEVICE IN TARGET DEVICE SELECTION CIRCUIT 203
S202
THE TARGET COMPARATOR CIRCUIT 204 COMPARES THE RESULT OF THE TARGET DEVICE SELECTION CIRCUIT 203 AND THE STATES OF THE TARGET OPERATING SIGNALS a 20 TO d 50 TO DETECT RESPONSES OF PLURAL PCI TARGET DEVICES
S203
S204
THE PCI DEVICE b 110 RESPONDS AS PCI TARGET DEVICE, WHILE THE PCI DEVICE D 130 ALSO RESPONDS AS PCI TARGET DEVICE, SO THAT ILLICIT OPERATION OCCURS ON THE PCI BUS 10
S302
STORE THE TWO PCI TARGET DEVICES WHICH RESPONDED TO THE ERROR STATUS CIRCUIT 205 AND THE PCI TARGET DEVICE SPECIFIED BY THE TARGET DEVICE SELECTION CIRCUIT 203
S105
REFER TO THE ERROR STATUS CIRCUIT 205 OF PCI BUS MONITOR CIRCUIT 200 TO VERIFY THAT THE PCI DEVICE d 130 RESPONDED ERRONEOUSLY
REPORT TO PROCESSOR UNIT 1 THAT PLURAL TARGET OPERATING SIGNALS ARE ACTIVATED
S205
MONITOR TARGET OPERATING SIGNALS
RECOVERY PROCESS
S106
REPORTS AN ERROR

FIG. 7

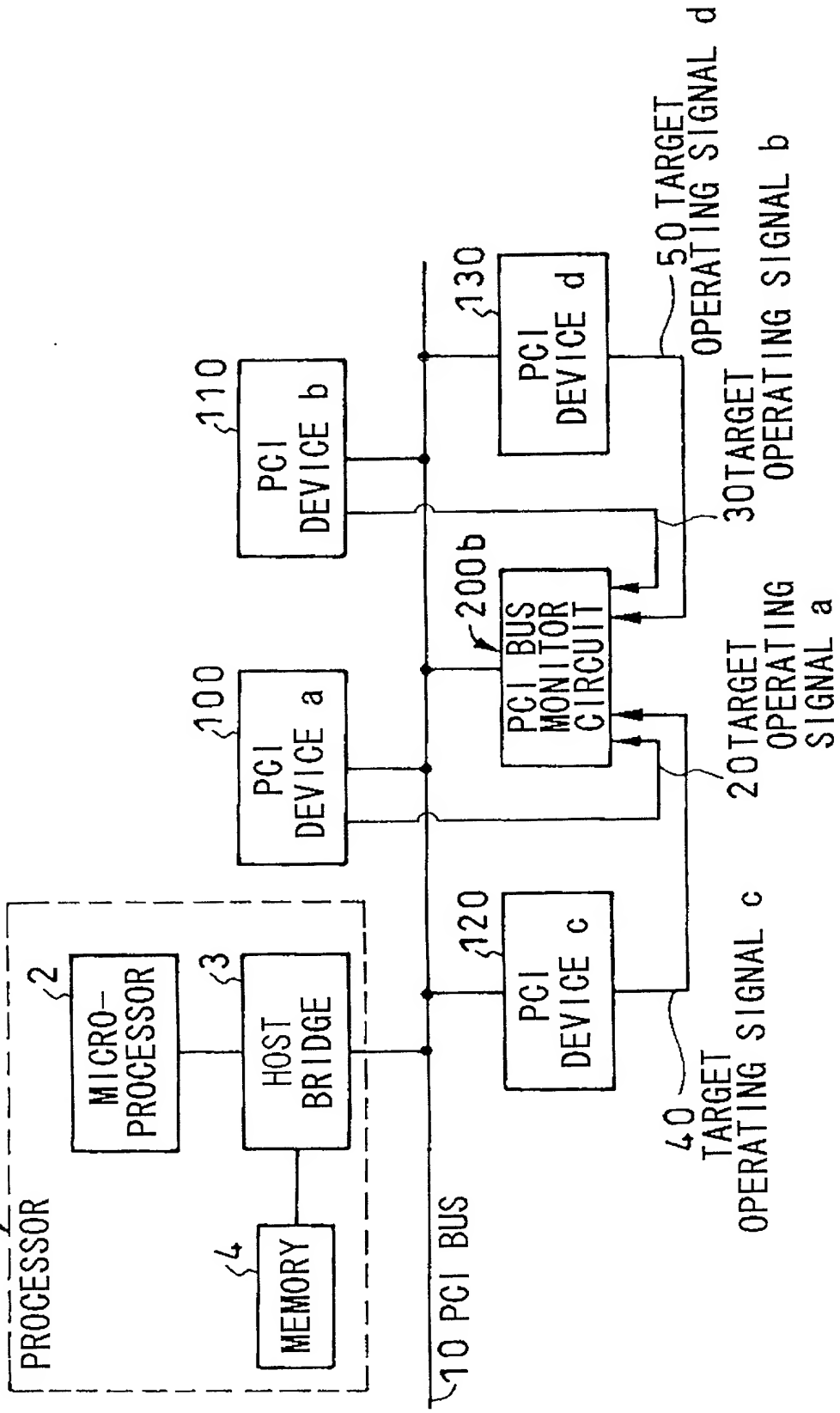

1
PROCESSOR
2
MICRO-PROCESSOR
3
HOST BRIDGE
4
MEMORY
10 PCI BUS
100
PCI DEVICE a
110
PCI DEVICE b
120
PCI DEVICE c
130
PCI DEVICE d
200b
PCI BUS MONITOR CIRCUIT
20 TARGET OPERATING SIGNAL a
30 TARGET OPERATING SIGNAL b
40 TARGET OPERATING SIGNAL c
50 TARGET OPERATING SIGNAL d

FIG. 8

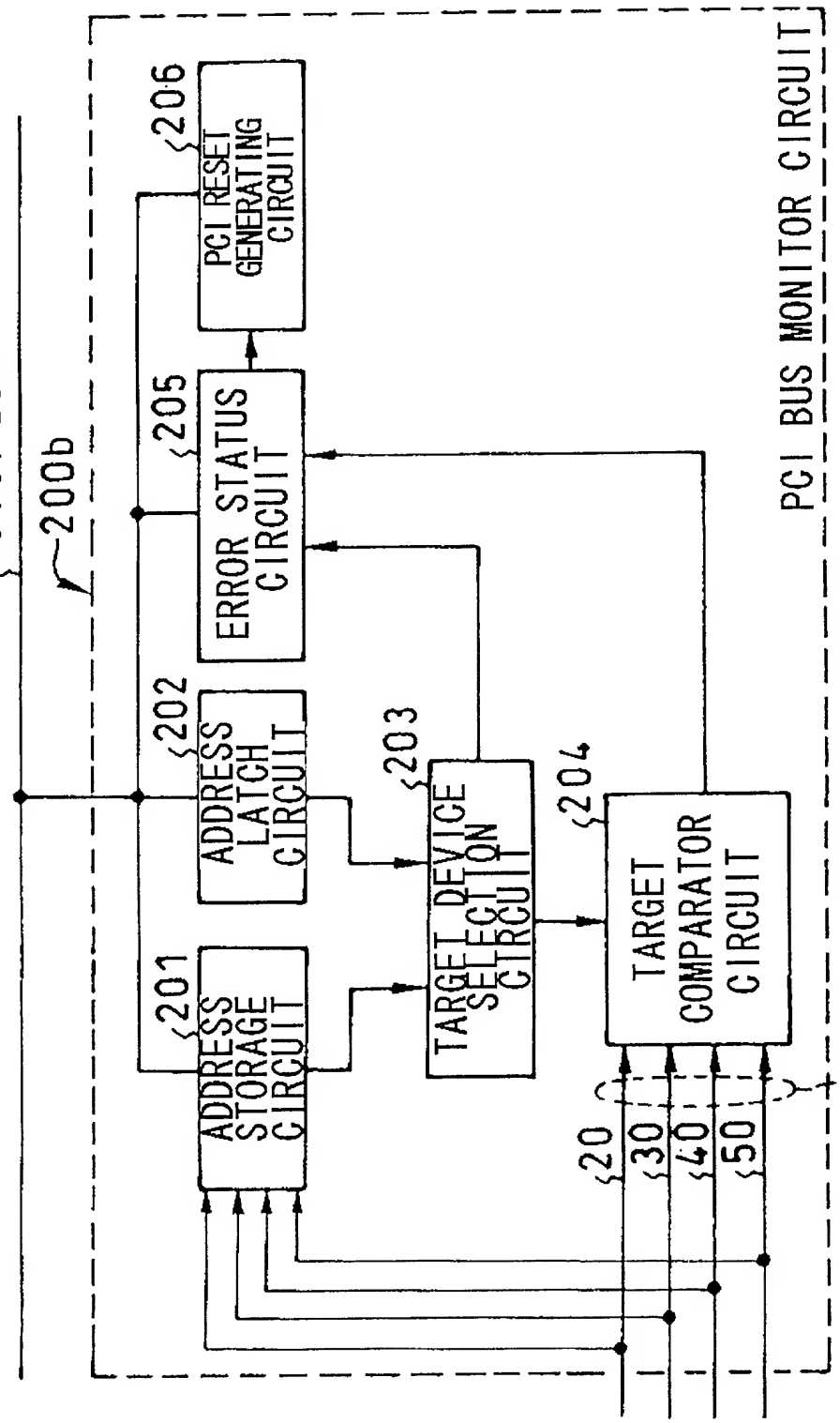

10 PCI BUS
200b
PCI BUS MONITOR CIRCUIT
206
PCI RESET GENERATING CIRCUIT
205
ERROR STATUS CIRCUIT
202
ADDRESS LATCH CIRCUIT
203
TARGET DEVICE SELECTION CIRCUIT
204
TARGET COMPARATOR CIRCUIT
201
ADDRESS STORAGE CIRCUIT
20
30
40
50
TARGET OPERATING SIGNALS a-d

FIG . 9

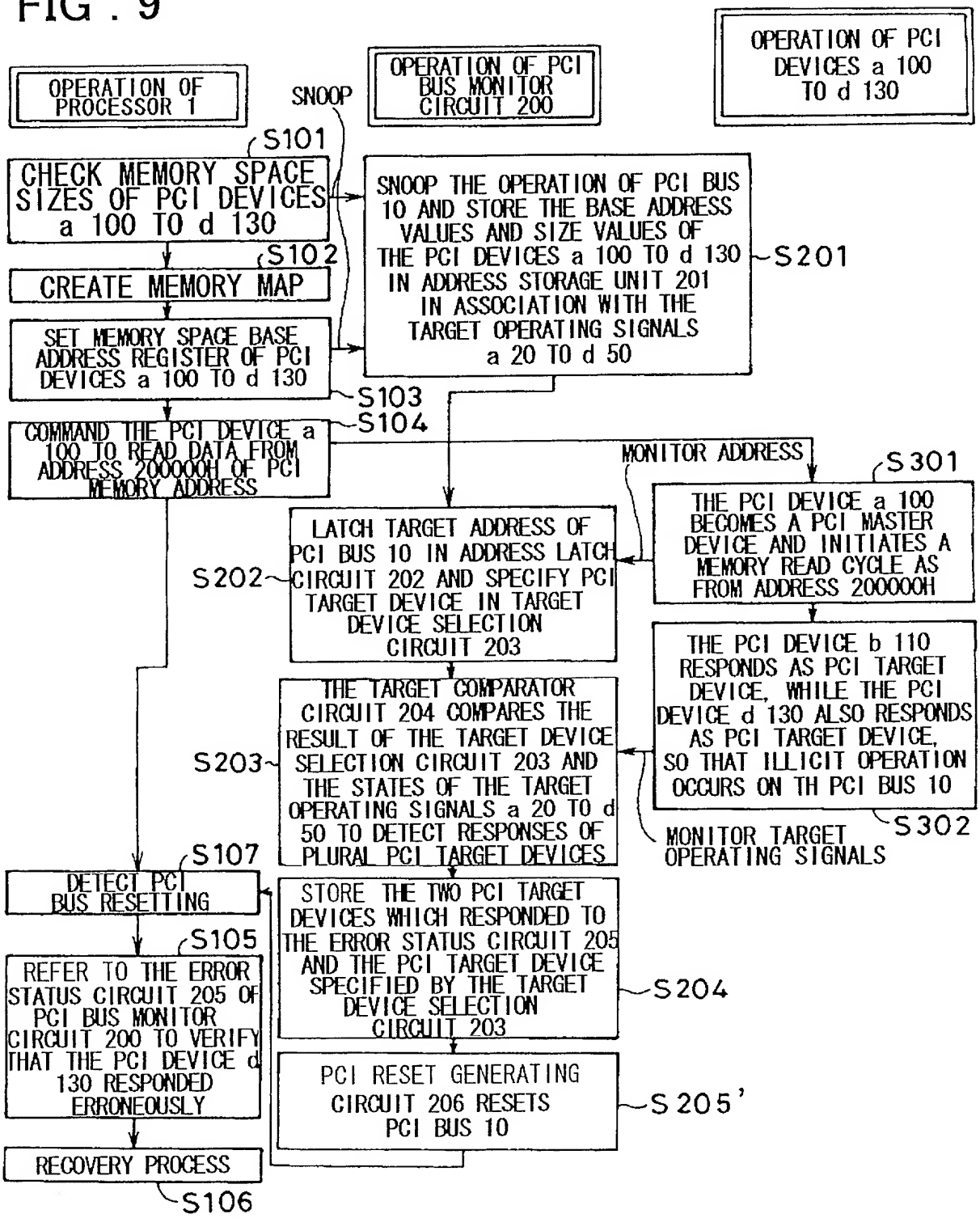

OPERATION OF PROCESSOR 1
SNOOP
OPERATION OF PCI BUS MONITOR CIRCUIT 200
OPERATION OF PCI DEVICES a 100 TO d 130
S101
CHECK MEMORY SPACE SIZES OF PCI DEVICES a 100 TO d 130
S102
CREATE MEMORY MAP
SET MEMORY SPACE BASE ADDRESS REGISTER OF PCI DEVICES a 100 TO d 130
S103
S104
COMMAND THE PCI DEVICE a 100 TO READ DATA FROM ADDRESS 200000H OF PCI MEMORY ADDRESS
SNOOP THE OPERATION OF PCI BUS 10 AND STORE THE BASE ADDRESS VALUES AND SIZE VALUES OF THE PCI DEVICES a 100 TO d 130 IN ADDRESS STORAGE UNIT 201 IN ASSOCIATION WITH THE TARGET OPERATING SIGNALS a 20 TO d 50
S201
MONITOR ADDRESS
S301
THE PCI DEVICE a 100 BECOMES A PCI MASTER DEVICE AND INITIATES A MEMORY READ CYCLE AS FROM ADDRESS 200000H
LATCH TARGET ADDRESS OF PCI BUS 10 IN ADDRESS LATCH CIRCUIT 202 AND SPECIFY PCI TARGET DEVICE IN TARGET DEVICE SELECTION CIRCUIT 203
S202
THE PCI DEVICE b 110 RESPONDS AS PCI TARGET DEVICE, WHILE THE PCI DEVICE d 130 ALSO RESPONDS AS PCI TARGET DEVICE, SO THAT ILLICIT OPERATION OCCURS ON TH PCI BUS 10
S302
THE TARGET COMPARATOR CIRCUIT 204 COMPARES THE RESULT OF THE TARGET DEVICE SELECTION CIRCUIT 203 AND THE STATES OF THE TARGET OPERATING SIGNALS a 20 TO d 50 TO DETECT RESPONSES OF PLURAL PCI TARGET DEVICES
S203
MONITOR TARGET OPERATING SIGNALS
S107
DETECT PCI BUS RESETTING
S105
REFER TO THE ERROR STATUS CIRCUIT 205 OF PCI BUS MONITOR CIRCUIT 200 TO VERIFY THAT THE PCI DEVICE d 130 RESPONDED ERRONEOUSLY
STORE THE TWO PCI TARGET DEVICES WHICH RESPONDED TO THE ERROR STATUS CIRCUIT 205 AND THE PCI TARGET DEVICE SPECIFIED BY THE TARGET DEVICE SELECTION CIRCUIT 203
S204
PCI RESET GENERATING CIRCUIT 206 RESETS PCI BUS 10
S205'
RECOVERY PROCESS
S106

FIG. 10

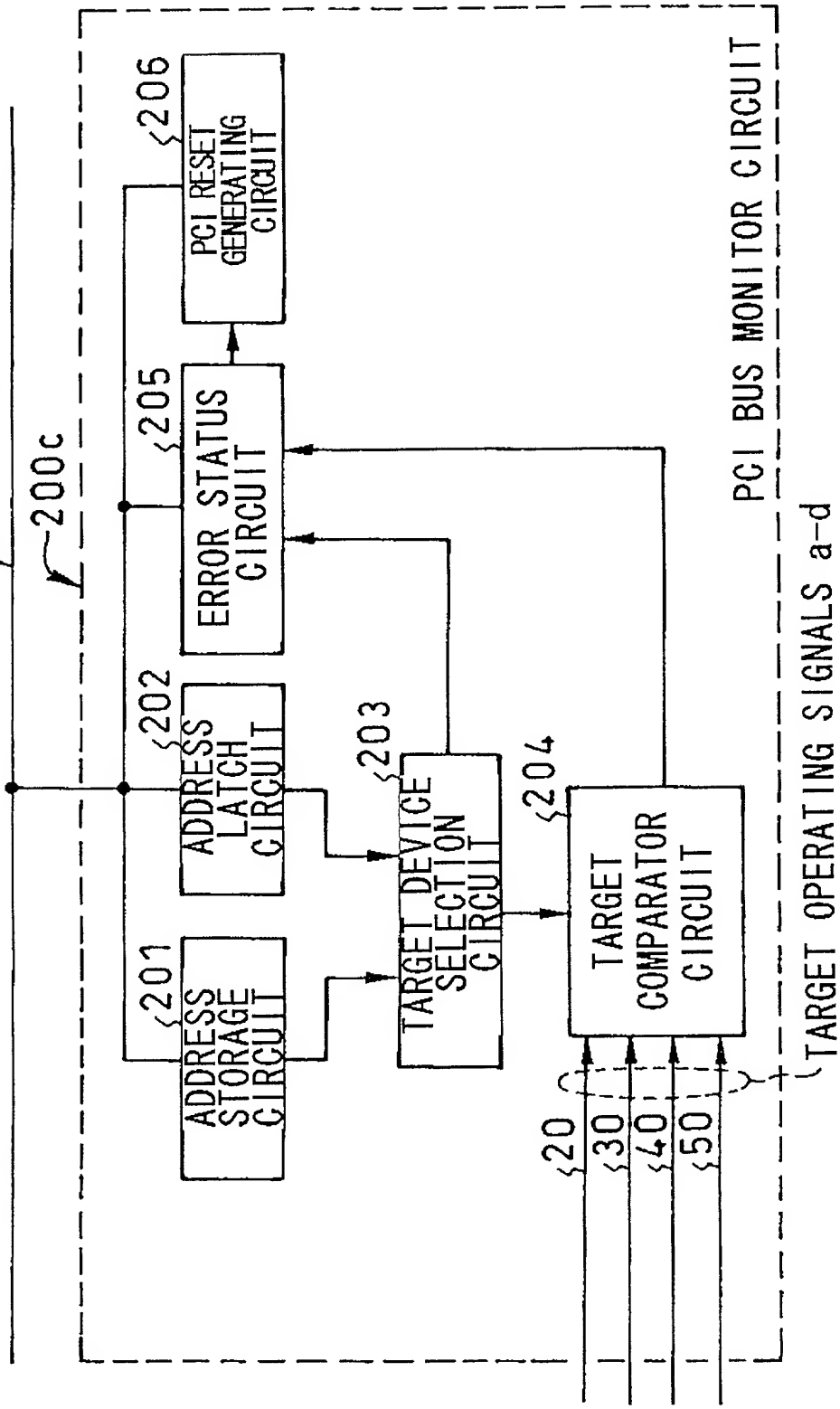

10 PCI BUS
200c
PCI BUS MONITOR CIRCUIT
206
PCI RESET GENERATING CIRCUIT
205
ERROR STATUS CIRCUIT
202
ADDRESS LATCH CIRCUIT
203
TARGET DEVICE SELECTION CIRCUIT
204
TARGET COMPARATOR CIRCUIT
201
ADDRESS STORAGE CIRCUIT
20
30
40
50
TARGET OPERATING SIGNALS a-d

FIG . 11

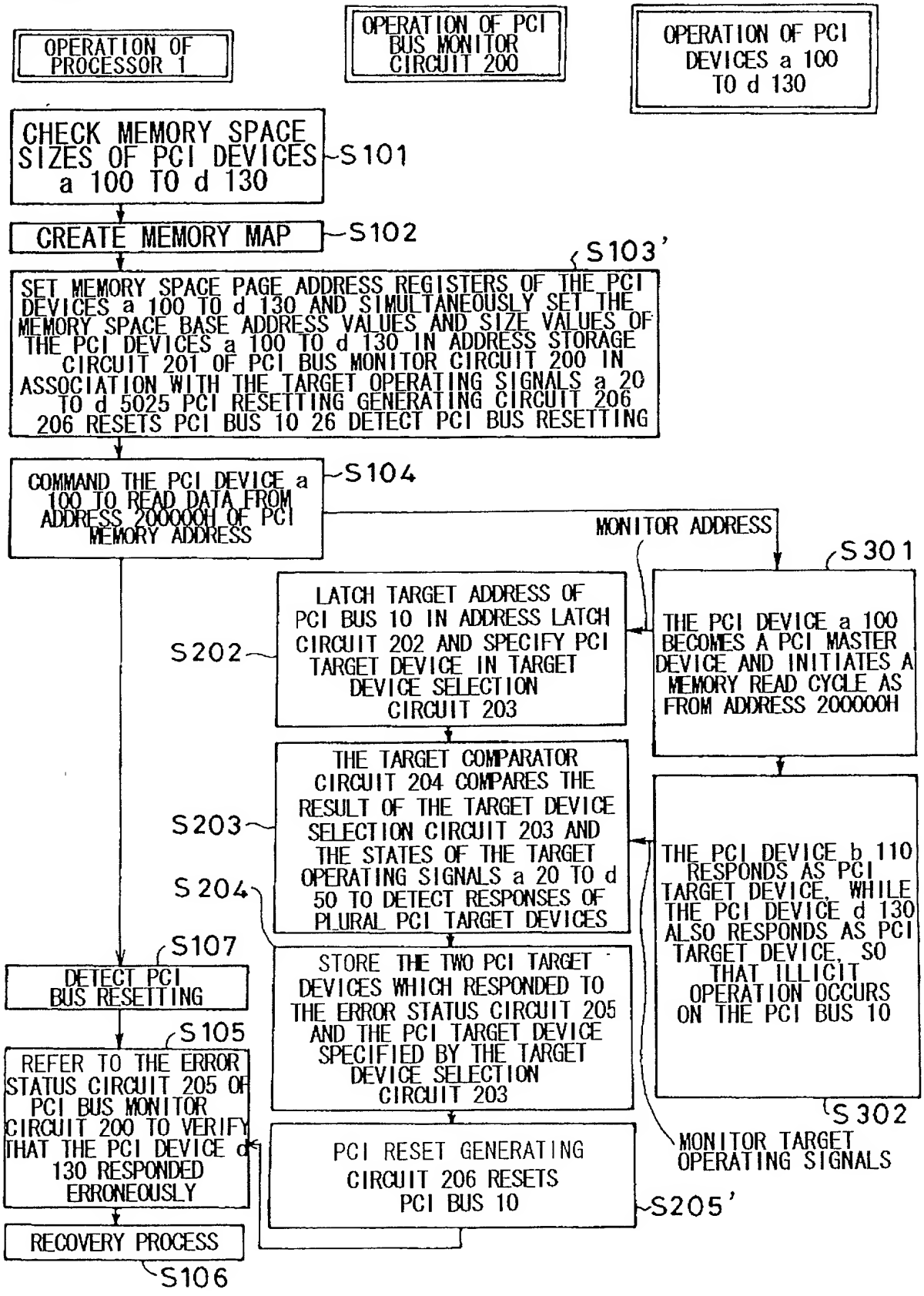

OPERATION OF PROCESSOR 1
OPERATION OF PCI BUS MONITOR CIRCUIT 200
OPERATION OF PCI DEVICES a 100 TO d 130
CHECK MEMORY SPACE SIZES OF PCI DEVICES a 100 TO d 130
S101
CREATE MEMORY MAP
S102
S103'
SET MEMORY SPACE PAGE ADDRESS REGISTERS OF THE PCI DEVICES a 100 TO d 130 AND SIMULTANEOUSLY SET THE MEMORY SPACE BASE ADDRESS VALUES AND SIZE VALUES OF THE PCI DEVICES a 100 TO d 130 IN ADDRESS STORAGE CIRCUIT 201 OF PCI BUS MONITOR CIRCUIT 200 IN ASSOCIATION WITH THE TARGET OPERATING SIGNALS a 20 TO d 5025 PCI RESETTING GENERATING CIRCUIT 206 206 RESETS PCI BUS 10 26 DETECT PCI BUS RESETTING
COMMAND THE PCI DEVICE a 100 TO READ DATA FROM ADDRESS 200000H OF PCI MEMORY ADDRESS
S104
MONITOR ADDRESS
S301
THE PCI DEVICE a 100 BECOMES A PCI MASTER DEVICE AND INITIATES A MEMORY READ CYCLE AS FROM ADDRESS 200000H
LATCH TARGET ADDRESS OF PCI BUS 10 IN ADDRESS LATCH CIRCUIT 202 AND SPECIFY PCI TARGET DEVICE IN TARGET DEVICE SELECTION CIRCUIT 203
S202
THE TARGET COMPARATOR CIRCUIT 204 COMPARES THE RESULT OF THE TARGET DEVICE SELECTION CIRCUIT 203 AND THE STATES OF THE TARGET OPERATING SIGNALS a 20 TO d 50 TO DETECT RESPONSES OF PLURAL PCI TARGET DEVICES
S203
S204
THE PCI DEVICE b 110 RESPONDS AS PCI TARGET DEVICE, WHILE THE PCI DEVICE d 130 ALSO RESPONDS AS PCI TARGET DEVICE, SO THAT ILLICIT OPERATION OCCURS ON THE PCI BUS 10
S302
MONITOR TARGET OPERATING SIGNALS
S107
DETECT PCI BUS RESETTING
STORE THE TWO PCI TARGET DEVICES WHICH RESPONDED TO THE ERROR STATUS CIRCUIT 205 AND THE PCI TARGET DEVICE SPECIFIED BY THE TARGET DEVICE SELECTION CIRCUIT 203
S105
REFER TO THE ERROR STATUS CIRCUIT 205 OF PCI BUS MONITOR CIRCUIT 200 TO VERIFY THAT THE PCI DEVICE d 130 RESPONDED ERRONEOUSLY
PCI RESET GENERATING CIRCUIT 206 RESETS PCI BUS 10
S205'
RECOVERY PROCESS
S106

FIG. 12

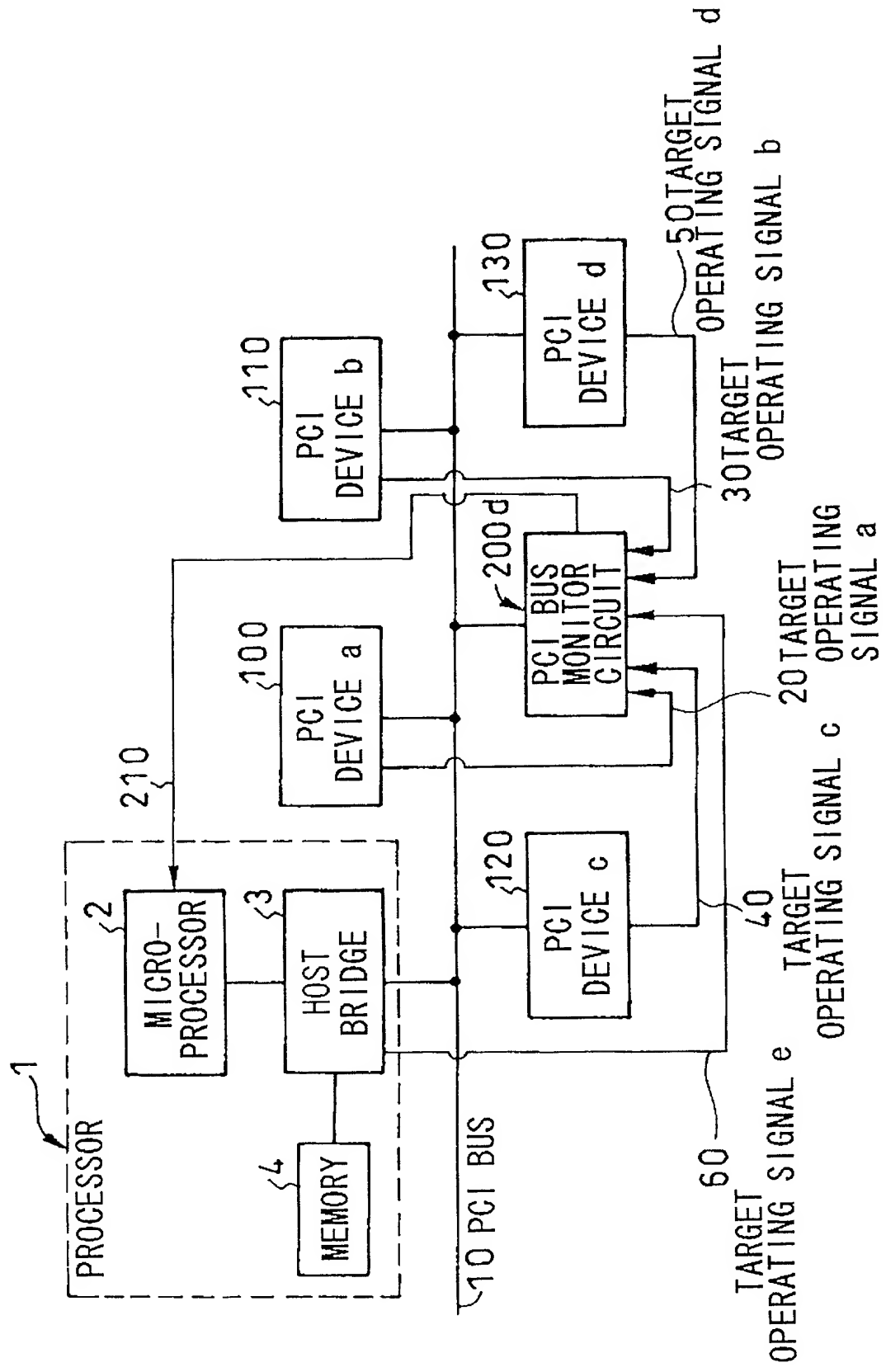

1
PROCESSOR
210
2
MICRO-PROCESSOR
3
HOST BRIDGE
4
MEMORY
10 PCI BUS
100
PCI DEVICE a
110
PCI DEVICE b
120
PCI DEVICE c
130
PCI DEVICE d
200d
PCI BUS MONITOR CIRCUIT
20 TARGET OPERATING SIGNAL c
30 TARGET OPERATING SIGNAL b
40 TARGET OPERATING SIGNAL a
50 TARGET OPERATING SIGNAL d
60 TARGET OPERATING SIGNAL e

FIG. 13

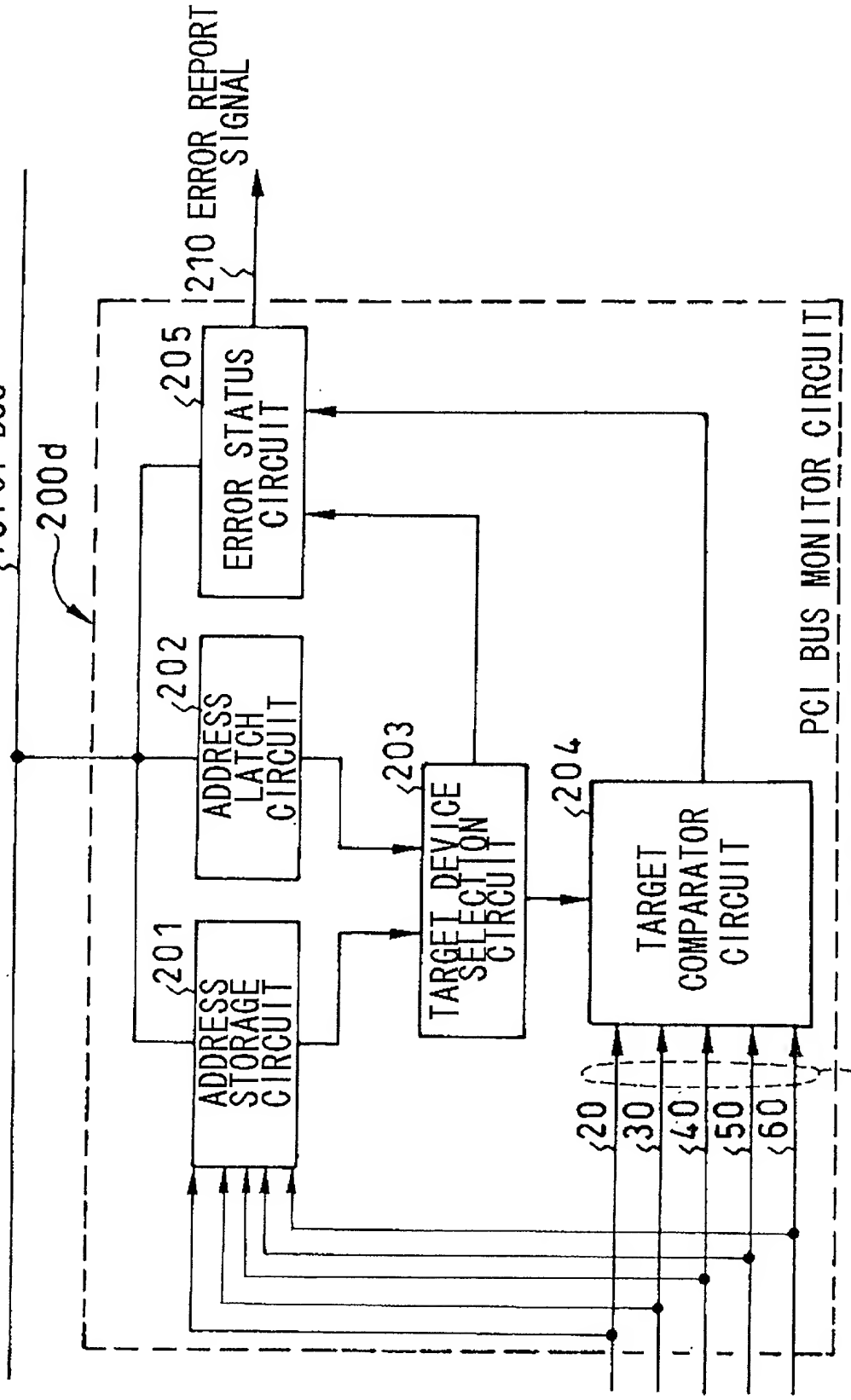

10 PCI BUS
200d
210 ERROR REPORT SIGNAL
205
ERROR STATUS CIRCUIT
202
ADDRESS LATCH CIRCUIT
203
TARGET DEVICE SELECTION CIRCUIT
204
TARGET COMPARATOR CIRCUIT
201
ADDRESS STORAGE CIRCUIT
PCI BUS MONITOR CIRCUIT
20
30
40
50
60
TARGET OPERATING SIGNALS a-e

FIG.14

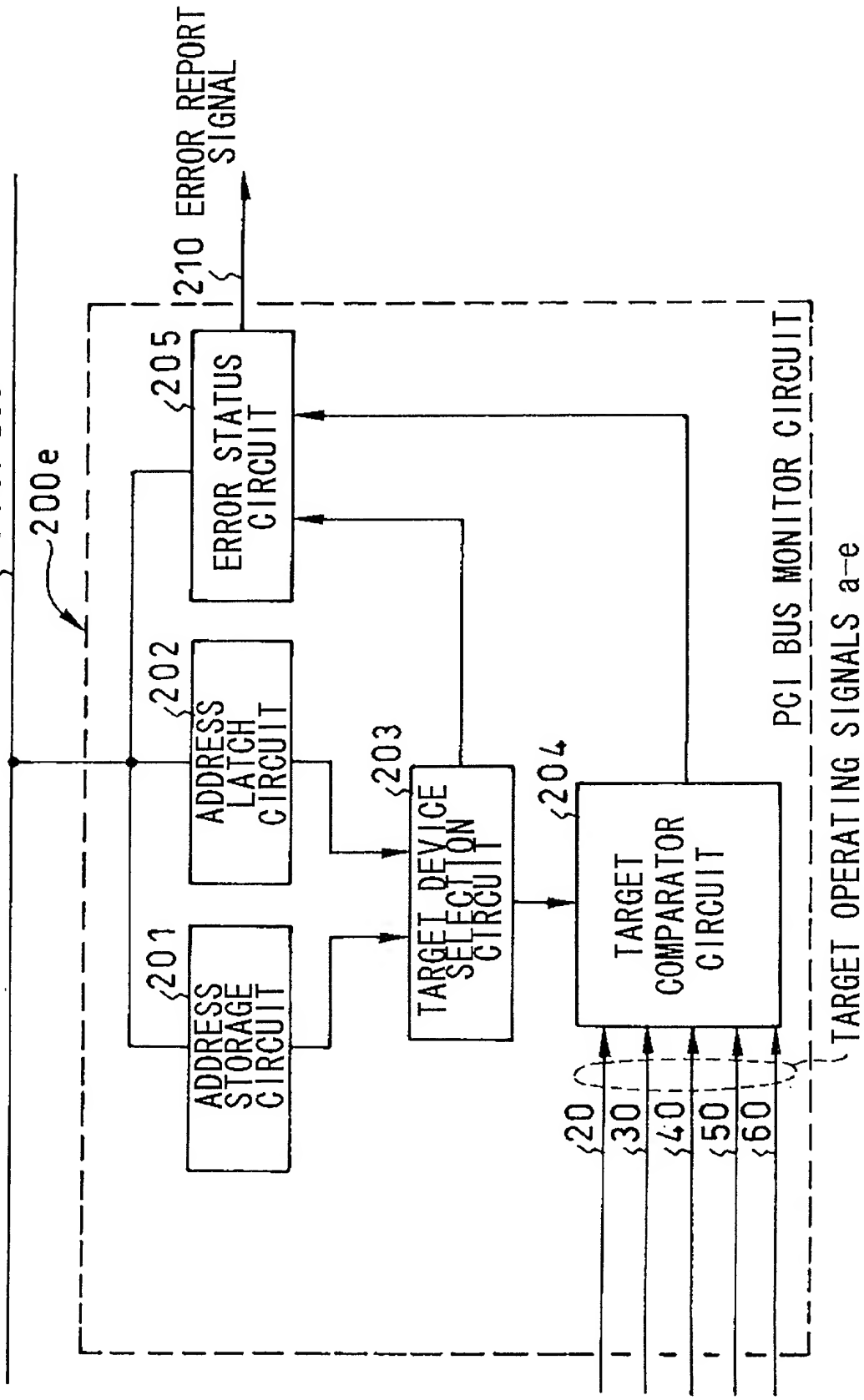

10 PCI BUS
200e
210 ERROR REPORT SIGNAL
205
ERROR STATUS CIRCUIT
202
ADDRESS LATCH CIRCUIT
201
ADDRESS STORAGE CIRCUIT
203
TARGET DEVICE SELECTION CIRCUIT
204
TARGET COMPARATOR CIRCUIT
PCI BUS MONITOR CIRCUIT
20
30
40
50
60
TARGET OPERATING SIGNALS a-e

FIG.15

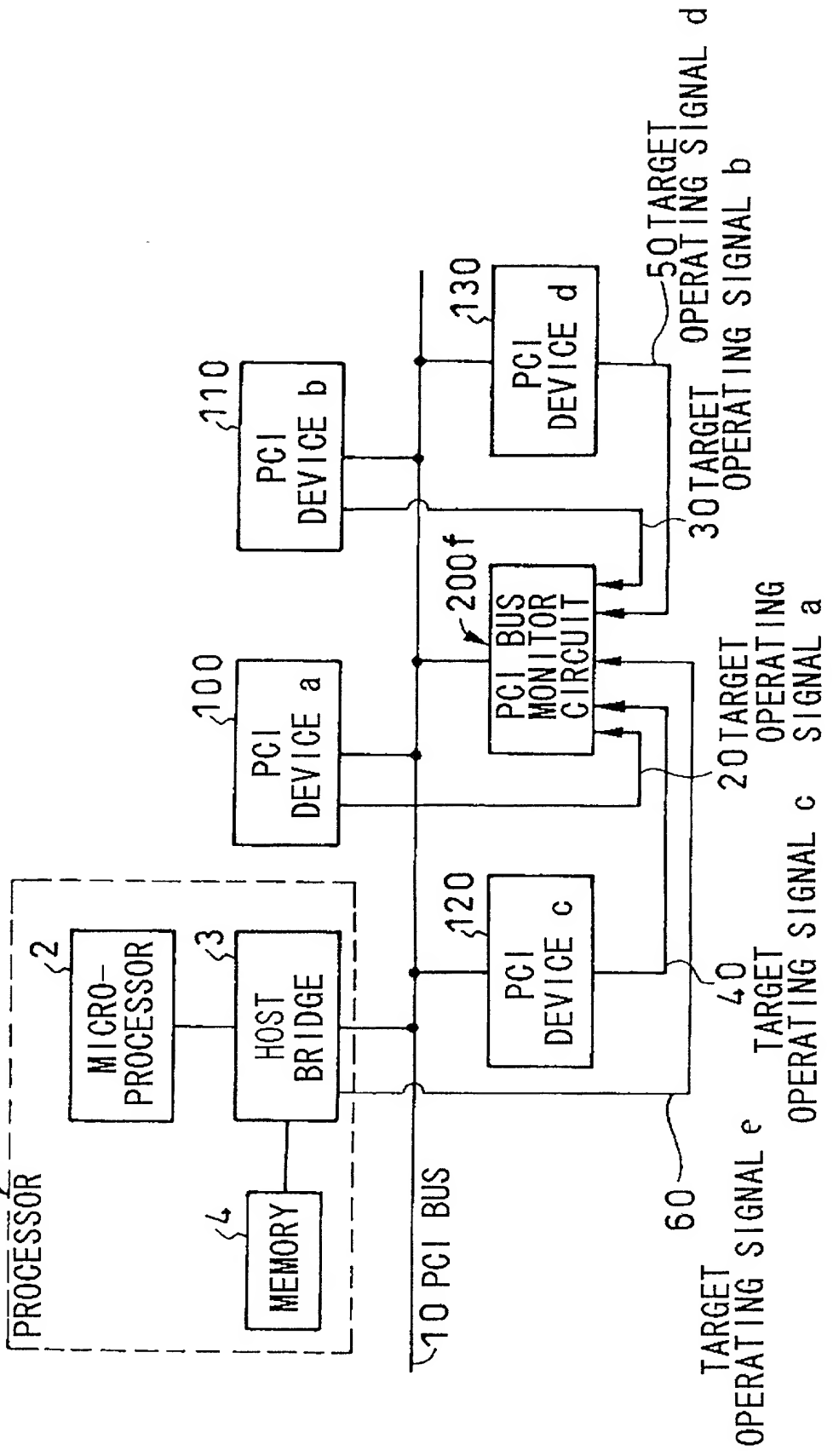

PROCESSOR
1
MICRO-PROCESSOR
2
HOST BRIDGE
3
MEMORY
4
10 PCI BUS
PCI DEVICE a
100
PCI DEVICE b
110
PCI DEVICE c
120
PCI DEVICE d
130
PCI BUS MONITOR CIRCUIT
200
60 TARGET OPERATING SIGNAL e
40 TARGET OPERATING SIGNAL c
20 TARGET OPERATING SIGNAL a
30 TARGET OPERATING SIGNAL b
50 TARGET OPERATING SIGNAL d

FIG. 16

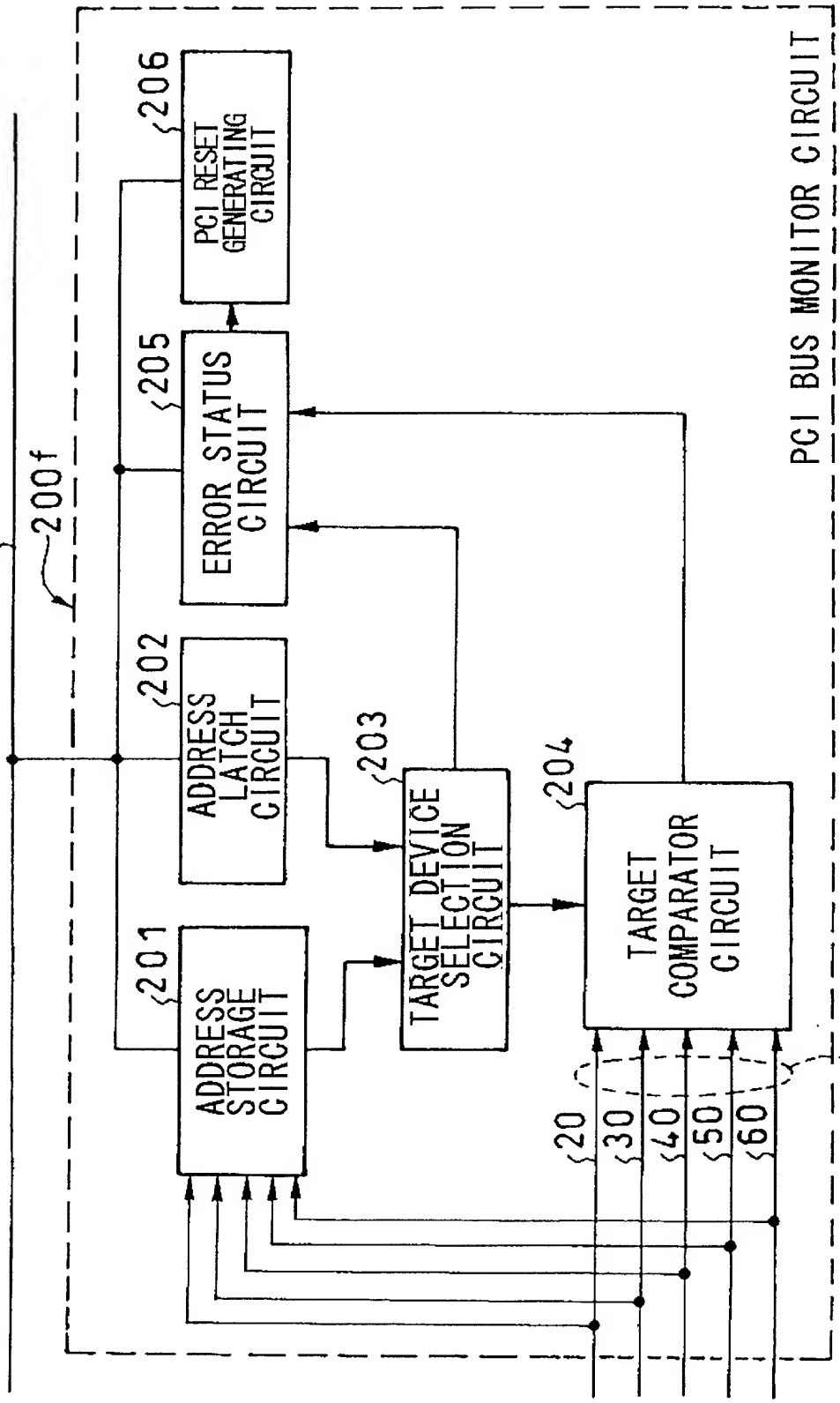
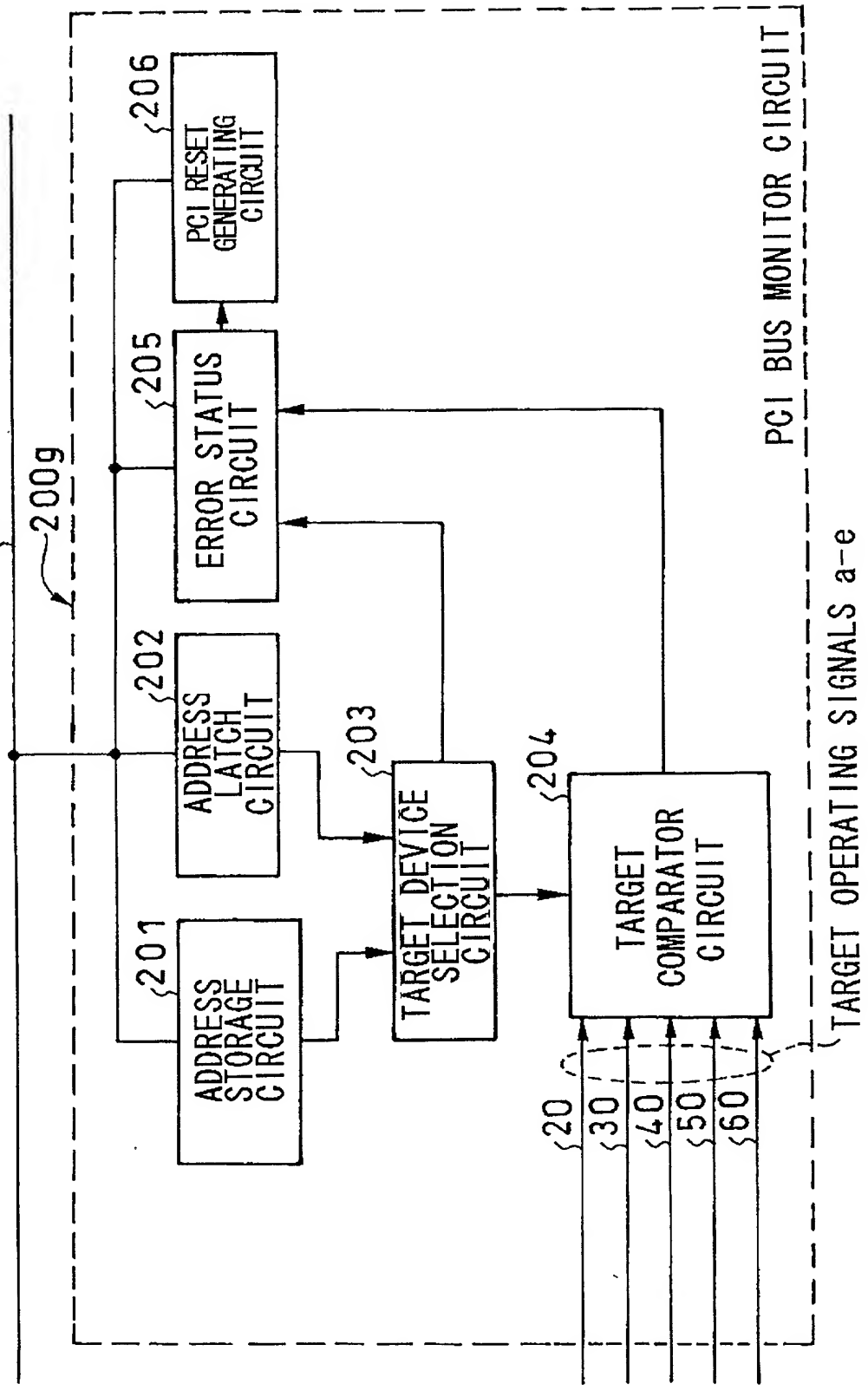

10 PCI BUS
200f
PCI BUS MONITOR CIRCUIT
206
PCI RESET GENERATING CIRCUIT
205
ERROR STATUS CIRCUIT
202
ADDRESS LATCH CIRCUIT
203
TARGET DEVICE SELECTION CIRCUIT
204
TARGET COMPARATOR CIRCUIT
201
ADDRESS STORAGE CIRCUIT
20
30
40
50
60
TARGET OPERATING SIGNALS a-e

FIG. 17


10 PCI BUS
200g
PCI BUS MONITOR CIRCUIT
206
PCI RESET GENERATING CIRCUIT
205
ERROR STATUS CIRCUIT
202
ADDRESS LATCH CIRCUIT
203
TARGET DEVICE SELECTION CIRCUIT
204
TARGET COMPARATOR CIRCUIT
201
ADDRESS STORAGE CIRCUIT
TARGET OPERATING SIGNALS a-e
20
30
40
50
60